REMARKS

Claims 1-12, 21-24, and 28-33 are all the claims presently being examined in the application. Claims 28-33 have been added to more completely define the invention.

Claims 1-12 and 21-24 stand rejected only on prior art grounds, and specifically under 35 U.S.C. § 102(e) as being anticipated by Joshi et al. (U.S. Patent No. 6,921,982), commonly assigned with the present application.

This rejection is respectfully traversed in view of the following discussion.

It is noted that any claim amendments herein are made only for more particularly pointing out the invention, and not necessarily for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements. Thus, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicant submits that all of the pending claims are patentable over the prior art of record.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (e.g., as exemplarily defined in independent claim 1) is directed to a semiconductor device, which includes a strained-silicon channel formed adjacent a source and a drain, a first gate formed over a first side of the channel,

a second gate formed over a second side of the channel, a first gate dielectric formed between the first gate and the strained-silicon channel, and a second gate dielectric formed between the second gate and the strained-silicon channel. The strained-silicon channel is non-planar.

Independent claim 21 recites a somewhat similar combination as claim 1, including "a strained-silicon channel formed adjacent a source and a drain; a first gate formed over a first side of said channel; a second gate formed over a second side of said channel. . . wherein said strained-silicon channel comprises a fin" (emphasis ours).

Such combinations of features are not taught or suggested by any of the piror art of record.

II. THE PRIOR ART REJECTION

Joshi US 6,921,982:

Joshi et al. Is fundamentally different from the claimed invention and indeed is irrelevant thereto.

Joshi et al. teaches a FET where the device channel 32 (e.g., see Fig. 4 and Figure 8F which shows a different view of the structure of Figure 4) is formed as a shell (envelope) 32 over a slab (core) 24. The core 24 and the shell (envelope) 32 are semiconductors with different natural lattice constants.

Per Joshi's teaching (Figures 2a and 2b) when the shell 32 is grown epitaxially over the core 24, the shell 32 will attempt to match the core's lattice constant and will form a strained layer (as illustrated by the example of strained silicon over Ge in Fig. 2b). As such, the "channel"

32 can have compressive or tensile strain based on the core 24 material. The FET can have from one to four gates (Figures 8A to 8D, gates labeled as 95 to 98).

The commonly used definition for a FinFET structure is the one used in Hu Chenming et al., U.S. Patent No. 6,413,802 entitled "FinFET transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture", which was briefly described in the Background section of the present application at page 1.

Using this widely accepted definition, a FinFET includes a thin silicon slab extending vertically from the substrate, with gates formed on the fin sidewalls. The fin serves as the FET channel and the gating of the carriers in the channel is achieved by the gates on each sides of the fin. To achieve a double-gate FET operation, the fin must be made very thin (less than 10 nm). With a thin fin, both gates control the device channel.

It is noted that, if the fin is made too wide, the device cannot be considered as a double-gate FET, but merely as two FETs in parallel. With a thick fin, a channel forms on the left sidewall and is solely gated by the left gate, and a second channel forms on the right sidewall and is solely gated by the right gate.

The present invention teaches a strained-channel semiconductor device (e.g., a FinFET). The device includes a thin strained-silicon channel 11 (e.g., a non-planar strained-silicon channel as defined by independent claim 1 or a fin as defined in claim 21) (all reference numerals used herein being exemplary and for the Examiner's clarity only and not for limiting the claims), a first gate dielectric 12 and a first gate conductor 13 on one sidewall of the fin, and a second gate dielectric 15 and a second gate conductor 16 on the opposite side of the fin (see Fig. 22 which

shows a cross-section of the present invention). As defined by new claims 28-29, the first gate conductor is electrically separated from the second gate conductor.

Joshi et al. does not teach or suggest a FinFET structure, let alone a structure as in the invention. For example, some fundamental structural differences and their implications are discussed below.

1. Joshi does not teach or suggest a FinFET structure as commonly defined by Hu Chenming (US 6,413,802). The structure taught by Joshi (e.g. Fig. 4) comprises a channel 32 (envelope), a gate 18 that is formed over the outer sidewall of the envelope 32, while the inner sidewall (28 or 30) of the envelope 32 is in contact with a core material 24. The core material 24 is not a gate!

   This structure does not form a double-gate FinFET since there is no second gate formed on the inner sidewall to control the channel. The gate material is only deposited on the outer surface of the "channel" (i.e., the envelope 32). As a result, the device taught by Joshi is merely a single-gate, non-planar strained-channel FET.

   Referring to independent claim 1 (and claim 21), Joshi does not teach or suggest "*a first gate formed over a first side of said channel and a second gate formed over a second side of said channel*".

   What is taught by Joshi is "*a first gate formed over a first side of said channel (32) and a core 24 material formed over a second side (surface 28) of the channel*". Surfaces 28 and 30 of Figure 4 (and similarly Figure 8F which shows a different view of the Figure 4 structure) are not coupled to a gate, but are coupled to a core material 24. That is, the surfaces 28 and 30 merely wrap around the core material 24. As a result, the

channel is only controlled from one surface (e.g., which is the outer surface of the envelope 32 on which gate 18 is deposited).

Thus, Joshi has the slab wrapped around the core 24 and only one surface of the core is being gated, not two! This structure of Joshi's is clearly distinguished from the claimed invention (see the cross section of Figure 22) which includes "*a first gate (13) formed over a first side of said channel (11) and a second gate (16) formed over a second side of said channel (11)*". Thus, in contrast to Joshi's Figure 4, the invention has a slab (channel) which is sandwiched between two (2) gates. This is not shown in Joshi.

It is noted that the above-mentioned structural difference is important and patentably significant. The two gates of the invention are important to the operation of the device and, if the two gates are not provided in the manner of the invention, then the device will not operate as intended, since the carriers to the channel will not be controlled as well with one gate as opposed to with two gates.

2. Secondly, in column 6, lines 3-13, Joshi defines the core 24 as silicon and the channel envelope 32 as SiGe for a P-FET. For an N-FET, the core 24 is selected as SiGe and the envelope (i.e., channel) 32 as Si. For both types of devices, the FET always comprises Si and SiGe. The presence of the SiGe in contact with the Si in the final structure is typically not desirable.

For example, the SiGe can lead to enhanced dopant diffusion when the source and drain junctions are formed. Additionally, due to bandgap alignment at the SiGe/Si heterojunction, it is possible for some of the carriers (holes) to form a parallel channel at the heterojunction in addition to the main channel at the gate-dielectric/Si interface. In view of the above problems, it is preferable that the final structure does not include SiGe. However, the structure proposed by Joshi requires the SiGe as a stressor to induce strain in the Si channel.

As clearly shown in Fig. 22 of the present application, as described in the present application and as claimed in new claim 31 (as well as in new dependent claims 32-33), the final structure does not include SiGe.

In the present application, SiGe is used as a sacrificial material to induce strain in the Si fin. The strained fin is firmly fixed by the gate material to the substrate, and then the SiGe stressor is removed. None of these features is taught or suggested by Joshi.

In view of all of the foregoing, independent claims 1 and 21 (as well as new independent claims 30-31) are not taught or suggested by Joshi et al.

Dependent Claims

The dependent claims are similarly allowable based not only on their dependency from their respective independent claims, but also for the additional limitations which they recite.

For example, turning to the limitations of dependent claim 4, Joshi indeed claims that the SiGe is "free from dislocation" (column 7, lines 18-20). However, to the best of the present

inventor's knowledge, experimental data does not support this claim. While implantation with hydrogen or helium following annealing may induce relaxation of SiGe films, the relaxation is achieved through the creation of misfit dislocation (i.e., "plastic relaxation" which is explained in the present application at pages 3-4, for example). For experimental evidence, see for example publications by J. Cai et al., "Strain relaxation and threading dislocation density in helium-implanted and annealed SiGe/Si(100) heterostructures", J. Appl. Phys., 95, 5347, (2004), and M. Luysberg,et al., "Effect of helium ion implantation and annealing on the relaxation behavior of pseudomorphic SiGe buffer layers on Si (100) substrates",J. Appl. Phys. 92, 4290, (2002). For the Examiner's convenience, copies of these references are included herewith.

Applicant, on the other hand, avoids plastic relaxation of SiGe by using an elastic relaxation technique as described in the specification on pages 3, 4, and 12.

Even if Joshi may indicate that the SiGe is free from dislocation, such a disclosure is not relevant to the invention, absent some clear teaching or suggestion of how to accomplish such a feature. Indeed, Joshi merely discloses a proposed result or benefit, but discloses or suggests no way of obtaining such a result/benefit. The above-mentioned references make clear that the structure of Joshi's which is allegedly "free from dislocation", may achieve relaxation but it is not going to be defect-free.

In reference to claim 6, Joshi claims that the gates can be independently controlled (column 10 line 12, figure 8F). However, no teaching is provided as to how that feature can be obtained.

In a true FinFET, the Fin width (i.e., spacing between gates 88 and 89), is less than 10 nm. With current lithographic technology, it would be near impossible to reliably define separate

contacts to gate 88 and 89. Indeed, there is absolutely no disclosure or suggestion of making the bar/slab 16 have a small width (i.e., narrow). As a result, Joshi is not forming a double-gate FinFET, but a structure having two (2) FETs in parallel. Again, gate 88 and 89 should be able to control a channel if the slab is thin enough.

However, there is no disclosure of forming the slab in such a manner, to allow both gates to control the channel, and as mentioned above current lithographic technology makes it near impossible to do so. There is no disclosure in Joshi of how to make contacts to the gates 88, 89 to the slab having a small width (gap) of 10 nm (100 angstroms). Joshi does not provide a solution for forming such a structure (other than perhaps accidentally!).

Thus, Joshi's gates are not independently controlled and again do not constitute a double-gate FinFET.

Regarding claim 10, Joshi does not disclose or suggest that the gates are self-aligned to the source and drain. Indeed, Figs. 3 and 8, which are the only figures showing the source and drain of the device, do not support a self-aligned source and drain to the gate. Additionally, there is no teaching of how to achieve a self-aligned source and drain to the gate.

That Joshi may (arguendo) teach that "islands are precision aligned" as alleged by the Examiner, is not relevant to the first and second gates of the invention being self-aligned to the source and drain. As is known in the art, "self-aligned" means that no other, additional alignment step is required, i.e., all alignment inherently results from the single alignment step/operation or is a product of the alignment. The Examiner is respectfully referred to Figure 3 of Joshi, in which there is a gate, source and drain, but these are not self aligned and certainly no scheme is disclosed of how the source and drain are aligned with respect to the gate.

In reference to claim 12, the Joshi structure is not planar as the fin stands above the plane of the wafer. While the structure of Fig. 8F may be more leveled than others structures showed in Joshi, it does not qualify as planar.

In contrast, the applicants are using several chemical mechanical polishing (CMP) steps in the fabrication of the device (see for examples transition from Fig. 9 to Fig 10, and Fig. 11 to Fig 12) to obtain a planarized structure. Thus, the invention does not merely provide one surface which is planar, but an overall planarized structure.

In view of all of the foregoing, Joshi fails to anticipate, or for that matter render obvious the claimed subject matter, either alone or in combination with any of the other prior art of record.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-12, 21-24, and 28-33, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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